First-Principles Molecular Dynamics Simulation of Oxide Layers for Radiation-Tolerant SiC Devices

Group Representative
Atsumi Miyashita Japan Atomic Energy Research Institute

Authors
Atsumi Miyashita *1 · Hideki Namba *1 · Masahito Yoshikawa *1 · Naoki Soneda *2
Toshiharu Ohnuma *2 · Takayuki Sakai *2 · Akiyuki Takahashi *2

*1 Japan Atomic Energy Research Institute
*2 Central Research Institute of Electric Power Industry
*3 Tokyo University of Science

Silicon carbide (SiC) has excellent physical properties, such as wide band gap and high-breakdown electric field, those are quite attractive for electronic devices with high-frequency or radiation-tolerant characteristics difficult to obtain by usual Si or GaAs semiconductors. The development of the formation technology of the SiO_2/SiC interface of high channel mobility and a high dielectric breakdown voltage is indispensable to improve SiC metal-oxide-semiconductor field effects transistors (MOSFETs) performance. Then, the relation between a physical structure and the electric characteristic of an interfacial defect is clarified, and the oxide film growth mechanism on the surface of the SiC crystal is clarified by generating the interfacial defect structure by using a first-principles molecular dynamics (MD) method, and calculating energy levels and the electric charge states, etc. When the heating and rapid cooling calculation is done by using the small-scale interface model of about 100 atoms, it was understood that the SiO_2 layer became amorphous structure when the heating temperature was 3000 K, heating time 3.0 ps and –1000 K/ps at the speed of rapid cooling. In this condition, the entire free energy has become smallest.

Keywords: SiC device, first-principles calculation, molecular dynamics, interfacial defect, rapid cooling

1. Introduction

Silicon carbide has excellent physical properties, such as wide band gap and high-breakdown electric field, those are quite attractive for electronic devices with high-frequency or radiation-tolerant characteristics difficult to obtain by usual Si or GaAs semiconductors. In addition, insulating layers of SiO_2 are easily obtained with thermal oxidization of SiC, which have superior dielectric properties good for the fabrication of MOSFETs. The MOSFETs, however, obtained on SiC substrates have less channel mobility in the inversion layers than theoretically expected; the reason is thought to be due to the defects generated thermally near the SiO_2/SiC interface, which are 100 times larger than those of Si MOS devices. The structures of SiO_2/SiC interface defects are partly clarified with physical measurement of SiO_2 layers on SiC, however, it is still insufficient. It is quite difficult to specify the relationship between the structures and experimentally obtained physical properties, i.e. electrical characteristics. A layer that is higher dielectric constant than SiC and SiO_2 that is called an interfacial interlayer exists in the SiO_2/SiC interface. In the inside of interlayer, it is known that there are many kinds of defects, which is Si dangling bond, C dangling bond, cluster of C that orbital changes into sp^2 hybrid, Si-Si bonding that occurs because C came off, atomic size void, etc. On the other hand, capacity-voltage (CV) method is often used for the measurement of an interfacial electric characteristic. A density of interfacial defects, energy levels, and the depth profile of oxide film etc. are clarified by the use of this method. However, the evaluation of an electric characteristic is difficult because the width of the band gap of the SiO_2/SiC interface is about three times the SiO_2/Si interface. Therefore, the defect evaluation over the entire band gap is hardly done. If an electric characteristic was able to be decided from the defect structure decided from a physical measurement or an interfacial physical structure was able to be decided according to the energy levels requested from an electric measurement, the relation between the oxidation method and the defect generation mechanism is easily examined, and the development of the interfacial formation method that makes MOSFETs the best electric characteristic becomes possible. We build up the SiO_2/SiC interface defect models and calculate the electrical characteristics such as the energy levels and charge states by using the first-principles MD. We derive the relationship

between the structures and the electrical characteristics and clarify the oxidation mechanisms near the SiO_2/SiC interface. Our final goal is to know the method for the fabrication of an interface with a low defect density for SiC MOSFETs.

2. Simulation result

2.1. Interface model and simulation technique

To simulate the characteristic of the SiC device accurately, it is necessary to reflect the SiO_2/SiC interfacial structure which controls an electric characteristic of the SiC device to the model in high precision. The SiO_2 layer of the SiC device is an amorphous SiO_2 structure made by oxidizing SiC. However, the electronic structure was calculated by using both SiO_2 and SiC crystal structures by limiting the calculation resource in the usual simulation [1]. When the crystal structure is used for SiO_2, the structure of the oxide film is different from an actual device. Only an abrupt interfacial structure is expressible and it is not realistic. In addition, it is not defective or there is an excessive defect in the interface of the crystal model. Then, we heat crystal SiO_2 to the high temperature, melt it, cool it rapidly, and make an amorphous SiO_2 structure in the simulation. A variety of kinds of defects are included in the SiO_2/SiC interface structure of an actual device, and an actual device characteristic can be simulated by emulating these defects. First of all, an atomic structural model by which crystal SiC and crystal SiO_2 are connected is made. Next, model that fixes the other side of interface in the SiC substrate is heated and cooled rapidly. As a result, the atoms in the SiC layer near the interface and in the SiO_2 layer can move, an amorphous SiO_2 structure is generated and relaxation occurs to an interfacial structure. As a result, it is thought that an interfacial structure that contains the defect in the condition similar to an actual device is obtained.

A first-principles MD method based on a density functional theory (DFT) was used for the model's heating and rapid cooling. At the calculation, we used a VASP (Vienna ab-initio Simulation Package) code which can be use ultrasoft Vanderbilt pseudopotentials (US-PP), the plane wave approximation, and the generalized gradient approximation (GGA) electron correlation. Because three-dimensional periodic boundary condition was used for the calculation, a vacuum part was taken above the SiO_2 layer to be able to neglect interaction with SiC layer on substrate side.

2.2. Optimization of analytical code

It seemed that the tuning in the Earth Simulator (ES) was not difficult because the vectorization code for SX-5 of NEC, and the parallel execution code that used MPI were included in the VASP code. However, the code for SX-5 was actually for single operation, and the MPI parallel execution code did not operate in the ES. Therefore, MPI parallel code had to be fixed that it was possible to operate in the ES environment. In addition, a time-consuming routine, for example 3D-FFT calculation, made a vectorization code by using the library for the ES, and to have executed the code at high speed. The vectorization ratio was the first about 60% and became 98.8% finally in the case of whole k space calculation mode in 452 atomic models; it was confirmed to obtain an almost enough vectorization ratio. As a result of the parameter tuning, the vectorization ratio has been improved up to 98% or more in Γ point only mode used to calculate MD. The entire execution speed had fallen for the inefficiency of the electronic distribution output routine. Then, the improvement of this routine reduced the elapsed time by half. However, it becomes parallelization ratio of 98.2% (parallelization efficiency ratio of 42.0%) by the result of the convergence calculation of 113 atomic models using 10 node 80 processors, it has not yet reached parallelization efficiency ratio of 50% and a further tuning is necessary.

2.3. Calculation of heating and rapid cooling simulation using small-scale model

To simulate an actual device structure, it is necessary to make an enough relaxed interfacial structure by using the model of the size of about at least 1000 atoms. It takes very long CPU time for the large scale model's simulation. In this year, we aimed to decide the parameter for the simulation of the large scale model by variously simulating a small-scale model of the size of about 100 atoms.

In the field of the SiC device research, the majority of the SiC substrate crystal used to research is 4H-SiC. Therefore, 4H-SiC structure was used for the model. The crystal plane used for the model is (0001) that is used for a lot of devices. The α quartz was used for the initial structure of SiO_2. The Si plane is used for the interface of SiC, and the SiC crystal and the SiO_2 crystal were arranged to become O of SiO_2 right above Si. In this case, O doesn't exist above one of three Si and dangling bond is generated. The lattice constant of the SiC crystal was used for the model. The end of SiC substrate was terminated by H. In the initial structure of 12 atomic layers of SiO_2 and 24 atomic layers of SiC. All layers of SiC and interfacial eight atomic layers of SiO_2 was assumed to be movable, and substrate side 16 atomic layers of SiC were fixed to the arrangement of the crystal structure.

Because the melting point of the SiO_2 crystal was about 2000 K, the heating temperature was changed from 2000 K to 4000 K and the process of changing into amorphous was observed. The heating time is 3.0 ps, and the rapid cooling speed is –1000 K/ps. Figure 1 shows the free energy change of the entire system when heating and rapid cooling. In the temperature from 2000 K to 3000 K, free energy in heating almost keeps constancy, and is thought to be a steady transi-

tion. An increase of free energy is seen a little in 3500 K, and it is thought that the system is not somewhat steady. In addition, an free energy of the system keeps increasing while heating it in 4000 K, it is thought that the system is completely unstable. Moreover, when the heating temperature was 3000 K, free energy after the system had been cooled became the lowest, i.e. the system was most steady. It seems that the heating temperature from 3000 K to 3500 K is suitable to make the system amorphous.

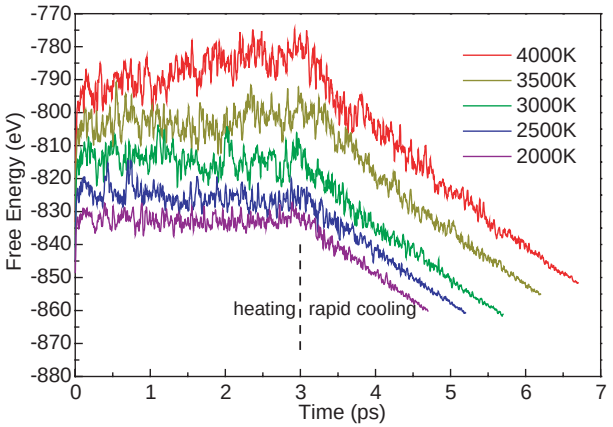

Fig. 1 Free energy in each heating temperature
The heating time is 3 ps, and the atoms were cooled down to the room temperature (300 K) with –1000 K/ps.

Next, the atomic structures after rapid cooling were compared at each temperature. Figure 2 shows the atomic structure. When the heating temperature was 4000 K, the system was guessed to be unstable from the calculation result of free energy, and the model separates by the interface when the calculation result of the atomic structure is seen, and it is regarded that the heating temperature is too high. When the heating temperature is 3500 K, the system is barely connected and the interface is very sparse. In addition, there are a lot of interfacial defects, and even the cluster structure of C-C-C exists, it is unsuitable to the simulation of the system with few interfacial defects. On the other hand, the cluster structure of C-C-C is observed at the interface in the transmission electron microscope image, it is thought that 3500 K result can simulate the actual SiO_2/SiC system when there are a lot of interfacial defects. When the heating temperature of 3000 K, though the SiO_2 structure has changed at random a

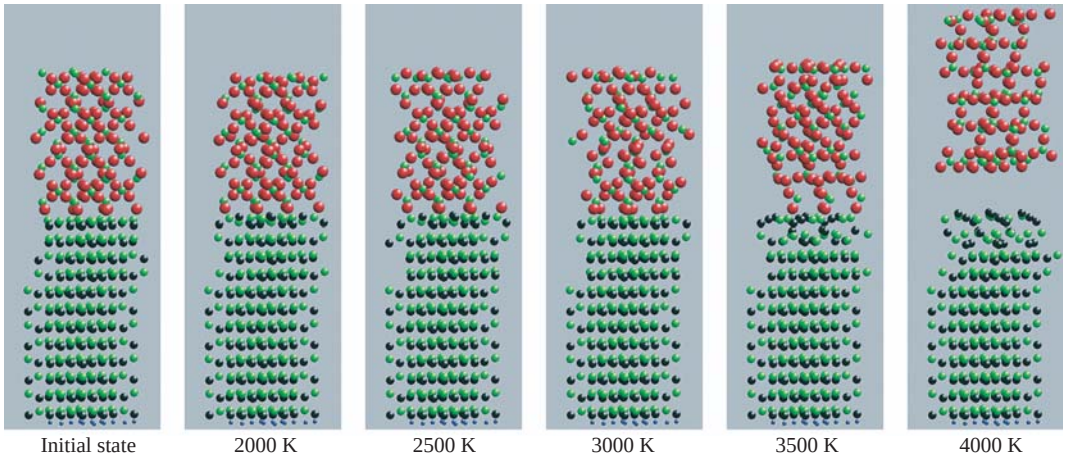

Fig. 2 Interfacial atomic structure after rapid cooling (Green:Si, Black:C, Red:O, Blue:H)

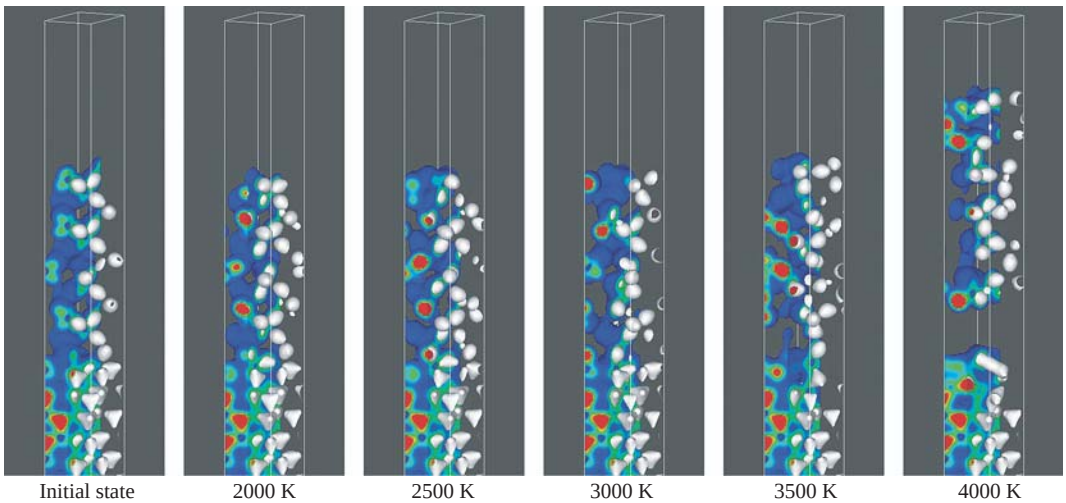

Fig. 3 Interfacial electronic density after rapid cooling

little, the interfacial structure has not changed from crystal SiO_2/SiC yet, and interfacial dangling bond is not canceled. It is uncertain whether this cause is the heating temperature is low and the heating time is short or a horizontal periodic condition is tight because of a small system. It is thought that this cause can be solved by the large-scale model calculation. The visualization image of the electronic density distribution in each step was made, and it was converted into animation image. Figure 3 shows an electronic density. From the animation image, it has been understood that the interface became sparse by the SiO_2 area shrinking when cooling in 3500 K. Moreover, in 4000 K, the entire SiO_2 area was not separate at a time but it separated while gradually flaking off from the surface.

3. Summary

The SiO_2/SiC interface structure was evaluated by using a first-principles MD method. When the heating and rapid cooling calculation is done by using the small-scale interface model of about 100 atoms, it was understood that the SiO_2 layer became amorphous when the heating temperature was 3000 K, heating time 3.0ps and –1000 K/ps at the speed of rapid cooling. In this condition, the entire free energy has become smallest, too. When the temperatures were lower than 3000 K, the SiO_2 layer became insufficient amorphous structure. When the temperatures were higher than 3000 K, it tended to take the oxidation layer part apart. From the above mentioned, to generate an amorphous SiO_2/SiC crystal structure, it is suitable to make the heating temperature about 3000 K.

References

[1] T. Ohnuma, H. Tsuchida, and T. Jikimoto. Submitted to Mat. Sci. Forum